ABSTRACT

The present invention relates to computer hardware and in particular to power management of high frequency storage designs, which are able to implement differential write or read access in a dynamic hardware arrangement of storage cells having some inner segmentation. More particularly, the present invention relates to a method and respective system of accessing memory cells within a dynamic hardware memory block operated with a bitline precharge circuit, in which differential read/ write access operations are performed by activating complementary bitlines. A reduction in power dissipation is realized by determining whether an access operation following a current access operation is a read or write access, and performing a precharge of the bitlines of the array only when a read operation follows the current access operation. A conventional precharge control signal (20) is combined with an external control signal (22) indicating if the next cycle is a read cycle. The combination of the two signals can be used, for example, as input to a simple AND gate to generate an effective precharge signal (24). The effective precharge signal permits precharging of bitlines only when those bitlines are used for read access in a respective next cycle. (Fig. 2)